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EXAMINER	
RANSOM, D	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/798,227	Applicant(s) Keeth
	Examiner David Ransom	Group Art Unit 2752

☒ Responsive to communication(s) filed on *Dec 15, 1998* .

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-24* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-24* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *AA-HG*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1 through 6, and 8 through 11 and 13 through 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. {US Patent number 5,577,236}.

The text not found in this section may be found in a prior office action.

4. Claims 20 through 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. {US Patent number 5,577,236}.

With respect to claim 20, Johnson discloses a method of adjusting data timing. This is taught as, "timing the internal operation of the modules **300***a*-**300***d*," at column 5 line 48 through

column 6 line 8. Johnson discloses in a memory system having a memory device. This is taught as memory bank **300**, at column 5 lines 15 to 33. Johnson discloses and a memory controller. This is taught as memory controller **302**, at column 5 lines 15 to 33. Johnson discloses establishing an initial output timing at the memory device. This is taught as read data from the sampling clock signals and the memory bank **300**, at column 6 lines 8 to 46. Johnson discloses transmitting a first digital signal. This is taught as, data read from the memory bank **300**, at column 6 lines 8 to 46. Johnson discloses from the memory device to the memory controller. This is taught as the memory bank **300** and the memory controller **302**, at column 6 lines 8 to 46. Johnson discloses according to the output timing. This is taught as data read from the memory bank **300**, at column 6 lines 8 to 46. "Which provides a delayed clock signal to a first receiver **319** via an output line **317**, to synchronize receipt by a latch **322** of read data from the memory bank **300** during the appropriate data valid window." Johnson discloses receiving the first digital signal. This is taught as data receipt by a latch, at column 6 lines 8 to 46. Johnson discloses identifying a phase difference of the received digital signal. This is taught as, "chosen to exhibit the sampling characteristics as the system clock signal on the signal line," and "receives a signal indicative of memory loading," at column 6 lines 18 to 46.

Johnson discloses relative to a timing reference signal. This is taught as, "the sampling clock signal selected by the clock selector **306** is fed, via output line **352**, to the delay module **313**, which coordinates the timing of receiving READ from the memory bank **300**," at column 6 line 47 through column 7 line 3. Johnson discloses transmitting an adjustment signal from the

memory controller to the memory device for revising the initial output timing. This is taught as command driver **308**, memory bank **300** and "command driver **308** that serves to initiate operations in the memory bank **300**," and "initiates operations in the memory bank **300**," at column 5 line 48 through column 6 line 46. Johnson discloses in response to the identified phase difference to produce a revised output timing. This is taught as, "the command driver **308** includes an input **309** for receiving the read command signals," and "which are conveyed to the memory bank **300**," at column 5 line 48 through column 6 line 46. Johnson discloses revising the initial output timing. This is taught as to synchronized receipt, at column 6 lines 8 to 46. Johnson discloses according to the adjustment signal. This is taught as delayed clock signals, at column 6 lines 8 to 18. Johnson discloses transmitting a second digital signal according to the revised output timing. This is taught as receive read data and command signals, at column 7 lines 21 to 40. "In response to the read command signals provided by the command driver **308**."

With respect to claim 21, Johnson discloses of the received first digital signal. This is taught as, "sampling clock signals comprise square wave signals," at column 8 lines 1 to 32. Johnson discloses generating a plurality of phase shifted signals. This is taught as clock signals **400** to **403**, at column 8 lines 1 to 32. Johnson discloses responsive to the timing references' signal. This is taught as with respect to clock signal, at column 8 lines 1 to 32. Johnson discloses comparing the first digital signal to each of the phase shifted signals. This is taught as correct sampling clock signal and sampling clock signal, at column 8 lines 1 to 32. Johnson discloses identifying one of the phase shifted signals. This is taught as clock selector selects, at column 8

lines 1 to 32. Johnson discloses having a phase within a selected range of phases. This is taught as clock signals **400** to **403**, at column 8 lines 1 to 32. Johnson discloses relative to the first digital signal. This is taught as coordinate timing of data read, at column 8 lines 1 to 32.

With respect to claim 22, Johnson discloses the steps of setting a delay of a delay circuit. This is taught as, "selection of approved sampling data," at column 7 lines 21 to 40. Johnson discloses and applying the timing reference to the delay circuit to produce the first digital signal. This is taught as appropriate sampling clock signals and to latch the read data, at column 7 lines 21 to 40. "Then, due to the selection of the appropriate sampling clock signal and the delays introduced by the delay module **313**."

With respect to claim 23, Johnson discloses the steps of storing data in an output register. This is taught as latch read data, at column 7 lines 21 to 40. Johnson discloses clocking the register with the first digital signal and outputting data from the register in response to the first digital signal. This is taught as appropriate sampling data and latch read data and appropriate sampling circuit, at column 7 lines 21 to 40.

With respect to claim 24, Johnson discloses the step of adjusting the delay of the delay circuit. This is taught as, "introduce a greater delay by the delay circuit," at column 9 lines 19 to 27.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7, 12 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. {US patent number 5,577,236} as applied to claim 6 above, and further in view of Smith {US Patent number 5,020,023}. The text not found here may be found in a prior office action.

Response to Arguments

7. Applicant's arguments filed December 15, 1999 have been fully considered but they are not persuasive.

The Applicant argues a method of adjusting data timing and controlling data flow in a memory system by revising the relative phase relationship between clock signals of the memory controller and clock signals of a memory device, assuming an initial output timing is established at the memory device. The memory device transmits to the memory controller data (either read data or an echo clock signal) based on the output timing. This is not persuasive because of the different phase characteristics created from the sampling clock in the memory controller being compared to an output signal or read data to correct timing deficiencies that may be apparent. This is apparent in Johnson column 6 lines 8 to 45. The controller is properly adjusted to capture

the data from the memory as the timing delay dictates for read operations. "The sampling clock signal is selected by the clock selector **306** is fed via the output line **352**, to the delay module **313**, which contains the timing of receiving Read from the memory bank **300**. (Johnson column 6 lines 47 to 50)

The Applicant argues the memory controller identifies any phase error of the transmitted signal relative to a clock signal in the memory controller and transmits some control data to be used by the memory device to revise the output timing that was initially established for subsequent data transmissions. This is not persuasive because of the different phase characteristics created from the sampling clock in the memory controller being compared to an output signal or read data to correct timing deficiencies that may be apparent. This is apparent in Johnson column 6 lines 8 to 45. The controller is properly adjusted to capture the data from the memory as the timing delay dictates for read operations. "The sampling clock signal is selected by the clock selector **306** is fed via the output line **352**, to the delay module **313**, which contains the timing of receiving Read from the memory bank **300**. (Johnson column 6 lines 47 to 50)

The Applicant argues the Johnson patent does not disclose where the memory controller identifies a phase error between a signal transmitted from the memory device and a clock signal of the memory controller, and then transmits data to the memory device in order to revise output timing according to the identified phase error. This is not persuasive because of the delay module on providing the second clock driver in the memory controller. "If the memory controller is implemented in an applications specific integrated circuit ("ASIC"), the second clock driver

automatically accounts for any variations in the process of manufacturing the memory controller, since the system clock driver and the second clock driver are constructed on the same chip using identical components. The delay module may also include supplementary delay unit." (Johnson, column 4 lines 16 to 21)

The Applicant argues there are no clock signals transmitted by the memory bank to the memory controller as with embodiments of the present invention. This is not persuasive because the memory device produces a timing signal from the memory that takes the form of a read data signal. "The appropriate module **300***a*-**300***d* places Read data onto the bus **320** in response to Read command signals provided by the command driver **308** on the command bus **349**, in accordance with the timing provided by the system clock circuit **303** via the system clock driver **301**. Then, due to the selection of the appropriate sampling clock signal and the delays introduced by the delay module **313**, the delayed clock signal provided on the line **317** enables the receiver **319** to present the appropriate clock signal to the latch **322** to latch the Read data received from the memory modules **300***a*-**300***d*." (Johnson, column 7 lines 29 to 40)

The Applicant argues the sampling clock signal selection in the Johnson system cannot be changed without physically changing switches or reprogramming a flash memory. Although the structure disclosed in the Johnson patent does not include a delay module, the delay value is fixed and cannot be modified without replacing the off-chip delay unit with a desired delay value. This is not persuasive because of the ability to vary the interval of the delay between successive clock circuits. "The predetermined delay of each sampling clock signal **400-403** with respect to the

system clock signal is preferably selected based on the expected levels of memory loading. With a wider variation of expected levels of memory loading, the interval of delay between successive sampling clock signals **400-403** will be greater." (Johnson, column 8 lines 10 through 15)

The Applicant argues claim 1 specifies a method of adjusting data timing in which the output timing at the memory device is initially determined and is the subsequently revised. The output timing is revised by first "transmitting an echo clock signal from the memory device to the memory controller according to the initial output timing." This is not persuasive because one of the use of the output timing to revise the memory controller's ability to latch the data through the use of a timing comparison with a signal from the memory bank. "Which provides a delayed clock signal to a first receiver **319** via an output line **317**, to synchronize the receipt by a latch **322** of Read data from the memory bank **300** during the appropriate data valid window." (Johnson, column 6 lines 14 to 18)

The Applicant argues after the echo clock signal is received at the memory controller, the memory controller identifies "a phase error of the received echo clock signal relative to the master clock signal" and "transmits control data to the memory device for revising the initial output timing in response to the identified phase error to produce a revised output timing." This is not persuasive because of the different phase characteristics created from the sampling clock in the memory controller being compared to an output signal or read data to correct timing deficiencies that may be apparent. This is apparent in Johnson column 6 lines 8 to 45. The controller is properly adjusted to capture the data from the memory as the timing delay dictates for read

operations. "The sampling clock signal is selected by the clock selector **306** is fed via the output line **352**, to the delay module **313**, which contains the timing of receiving Read from the memory bank **300**. (Johnson column 6 lines 47 to 50)

The Applicant argues thereafter, the memory device revises the initial output timing to transmit a second set of data to the memory controller according to the revised output timing. This is not persuasive because the memory device produces a timing signal from the memory that takes the form of a read data signal. "The appropriate module **300***a*-**300***d* places Read data onto the bus **320** in response to Read command signals provided by the command driver **308** on the command bus **349**, in accordance with the timing provided by the system clock circuit **303** via the system clock driver **301**. Then, due to the selection of the appropriate sampling clock signal and the delays introduced by the delay module **313**, the delayed clock signal provided on the line **317** enables the receiver **319** to present the appropriate clock signal to the latch **322** to latch the Read data received from the memory modules **300***a*-**300***d*." (Johnson, column 7 lines 29 to 40)

The Applicant argues as explained above, the system disclosed in the Johnson Patent does not include a memory device that transmits an echo clock signal (not only read data) to a memory controller according to an initial output timing. This is not persuasive because the memory device produces a timing signal from the memory that takes the form of a read data signal. "First, a system clock circuit is provided to clock the read commands into the memory bank **300**." (Johnson column 5 lines 49 through 50) "The appropriate module **300***a*-**300***d* places Read data onto the bus **320** in response to Read command signals provided by the command driver **308** on

the command bus **349**, in accordance with the timing provided by the system clock circuit **303** via the system clock driver **301**. Then, due to the selection of the appropriate sampling clock signal and the delays introduced by the delay module **313**, the delayed clock signal provided on the line **317** enables the receiver **319** to present the appropriate clock signal to the latch **322** to latch the Read data received from the memory modules **300***a*-**300***d*." (Johnson, column 7 lines 29 to 40)

The Applicant argues claims 6 and 16 specifies that the memory device produces and transmits an echo signal in response to a first (second) read command and the memory controller compares the received echo signal to a master clock signal to select an adjusted time delay. Then the memory device then responds to a second (third) read command by transmitting a second set of data to the memory controller with the adjusted time delay. This is not persuasive because the memory device produces a timing signal from the memory that takes the form of a read data signal. "The appropriate module **300***a*-**300***d* places Read data onto the bus **320** in response to Read command signals provided by the command driver **308** on the command bus **349**, in accordance with the timing provided by the system clock circuit **303** via the system clock driver **301**. Then, due to the selection of the appropriate sampling clock signal and the delays introduced by the delay module **313**, the delayed clock signal provided on the line **317** enables the receiver **319** to present the appropriate clock signal to the latch **322** to latch the Read data received from the memory modules **300***a*-**300***d*." (Johnson, column 7 lines 29 to 40)

The Applicant argues claim 10 is directed to a memory controller producing echo signals in response to master clock signals on to a clock bus from a master clock source in the memory

controller. A phase comparing circuit produces a phase signal in response to a phase difference between the echo signal and the master clock signal. A logic circuit that produces adjustment data in response to the phase signal and a control data circuit adapted to produce a command signal in response to the adjustment data. This is not persuasive because the memory device produces a timing signal from the memory that takes the form of a read data signal. "First, a system clock circuit is provided to clock the read commands into the memory bank **300**." (Johnson column 5 lines 49 through 50) "The appropriate module **300***a*-**300***d* places Read data onto the bus **320** in response to Read command signals provided by the command driver **308** on the command bus **349**, in accordance with the timing provided by the system clock circuit **303** via the system clock driver **301**. Then, due to the selection of the appropriate sampling clock signal and the delays introduced by the delay module **313**, the delayed clock signal provided on the line **317** enables the receiver **319** to present the appropriate clock signal to the latch **322** to latch the Read data received from the memory modules **300**a-**300**d." (Johnson, column 7 lines 29 to 40) "In particular, one of the sampling clock signals from the sampling clock circuit is selectively fed to a delay module **313**, which provides a delayed clock signal to a first receiver." "The sampling clock signal selected by the clock selector **306** is fed, via output line **352**, to the delay module **313**, which coordinates the timing of receiving Read from the memory bank **300**." (Johnson, column 6 lines 47 to 50)

The Applicant argues claim 13 further specifies that the memory controller includes a phase comparator that produces an adjust command responsive to a phase difference between a

master clock signal from a master clock generator and an echo signal from the echo signal generator. This is not persuasive because the memory device produces a timing signal from the memory that takes the form of a read data signal. "First, a system clock circuit is provided to clock the read commands into the memory bank **300**." (Johnson column 5 lines 49 through 50) "The appropriate module **300***a*-**300***d* places Read data onto the bus **320** in response to Read command signals provided by the command driver **308** on the command bus **349**, in accordance with the timing provided by the system clock circuit **303** via the system clock driver **301**. Then, due to the selection of the appropriate sampling clock signal and the delays introduced by the delay module **313**, the delayed clock signal provided on the line **317** enables the receiver **319** to present the appropriate clock signal to the latch **322** to latch the Read data received from the memory modules **300***a*-**300***d*." (Johnson, column 7 lines 29 to 40) "In particular, one of the sampling clock signals from the sampling clock circuit is selectively fed to a delay module **313**, which provides a delayed clock signal to a first receiver." "The sampling clock signal selected by the clock selector **306** is fed, via output line **352**, to the delay module **313**, which coordinates the timing of receiving Read from the memory bank **300**." (Johnson, column 6 lines 47 to 50)

The Applicant argues the Johnson system does not have a phase comparing circuit comparing the phase difference between a signal transmitted by the memory device and a clock signal of the memory controller. The system shown does not include a phase comparing circuit that compares the phase error between a clock signal transmitted from the memory bank to the memory controller or a logic circuit that produces a signal in response to the output of the phase

comparing circuit. This is not persuasive because the memory device produces a timing signal from the memory that takes the form of a read data signal. "First, a system clock circuit is provided to clock the read commands into the memory bank **300**." (Johnson column 5 lines 49 through 50) "The appropriate module **300***a*-**300***d* places Read data onto the bus **320** in response to Read command signals provided by the command driver **308** on the command bus **349**, in accordance with the timing provided by the system clock circuit **303** via the system clock driver **301**. Then, due to the selection of the appropriate sampling clock signal and the delays introduced by the delay module **313**, the delayed clock signal provided on the line **317** enables the receiver **319** to present the appropriate clock signal to the latch **322** to latch the Read data received from the memory modules **300***a*-**300***d*." (Johnson, column 7 lines 29 to 40) "In particular, one of the sampling clock signals from the sampling clock circuit is selectively fed to a delay module **313**, which provides a delayed clock signal to a first receiver." "The sampling clock signal selected by the clock selector **306** is fed, via output line **352**, to the delay module **313**, which coordinates the timing of receiving Read from the memory bank **300**." (Johnson, column 6 lines 47 to 50)

The Applicant argues additional delay of the selected clock signal is possible only by inserting a fixed, off-chip delay unit into the signal path or replacing that fixed delay unit with another fixed delay unit having a different delay value. This is not persuasive because of the ability to adjust the phase values and the need to provide either an on-chip delay circuit or an off-chip delay circuit are for reasons other than the purpose of changing magnitude. "With a wider

variation of expected memory loading, the interval of delay between successive sampling clock signals **400-403** will be greater." (Johnson, column 8 lines 13 through 15) The ability to modify the delay based on loading, provides an effective way to allow for frequent changes if not automatic changes in the control of the phase difference. "If the memory controller is implemented in an ASIC, the delay unit **316**, preferably comprises an 'off-chip' device to provide added flexibility in adjusting the delay unit **316**, and to ensure that the delay unit **316** is independent of any process variations experienced by the components of the ASIC." (Johnson column 6 lines 61 through 66) Flexibility is improved with the off-chip delay module, but flexibility is not lost in a on-chip device for the delay module.

The Applicant argues claims 7 and 19 add the limitation of adjusting a vernier to select the adjusted time delay. After the memory device transmits an echo clock signal to the memory controller, the echo clock signal and the master clock signal are compared to determine their relative phase difference. Adjustment of the vernier is made based on the relative phase error determined from the comparison. This is not persuasive because of the time delay and vernier skew provided in Smith columns 5 and 10. "If it is known that a particular data item is to be transmitted at local time **45** and the skew is three with a propagation delay of from one to three, then the item might not be available at the receiver until local time **52**." (Column 5 lines 26 through 30) "The arrangement is similar for outgoing transmissions as indicated in FIG. 9B except that there is only one stage which requires Vernier Skew compensation." (Column 10 lines 50 to 52)

The Applicant argues claim 12 describes the memory controller as having a signal source that includes a multiple delay-locked loop. This is not persuasive because Jeddeloh provides the defining characteristics for a multiple phase-locked-loops or delays in an ASIC device. "This form of skew is often handled by making the signal lengths between the chips and the signal source the same, and/or by measuring the delays to the different chips and compensating for the delays using phase locked loops or inserted delays." (Jeddeloh, column 1 lines 37 through 41)

The Applicant argues Smith's use of "vernier" has nothing to do with disclosing or suggesting adjusting a vernier in adjusting a time delay in response to the relative phase relationship between two signals. This is not persuasive because of the time delay and vernier skew provided in Smith columns 5 and 10. "If it is known that a particular data item is to be transmitted at local time **45** and the skew is three with a propagation delay of from one to three, then the item might not be available at the receiver until local time **52**." (Column 5 lines 26 through 30) "The arrangement is similar for outgoing transmissions as indicated in FIG. 9B except that there is only one stage which requires Vernier Skew compensation." (Column 10 lines 50 to 52)

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any response to this action should be mailed to:
Commissioner of patents and trademarks
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or faxed to: (730)308-9051 (for formal communications intended for entry) or (703)308-9051 (for informal or draft communications, please label "PROPOSED" or "DRAFT"); Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA 22209, sixth floor receptionist.

Any inquiry concerning this communication should be directed to David Ransom at telephone number (703) 305-4035. The examiner can normally be reached on Monday through Friday from 9:00 to 5:00. If there is any problem contacting me call John Cabeca at (703)308-3116. The fax number to this office is (703)308-5357.

Any inquiry of a general nature or relating to the status of this applications or proceeding should be directed to the group receptionist whose telephone number is (703)305-3900.

David Ransom
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